WHAT IS CLAIMED IS:

1. A receiver circuit comprising:

an oscillator circuit configured to generate a calibration tone and a phase locked loop (PLL) reference signal;

a phase locked loop circuit configured to generate a PLL output signal that is phase locked in relation to the PLL reference signal;

a quadrature generator configured to generate quadrature mixer local oscillator (LO) signals derived from the PLL output signal; and

an in-phase/quadrature (IQ) mixer configured to mix the calibration tone with the quadrature mixer LO signals.

2. The receiver circuit as recited in Claim 1, wherein the oscillator circuit includes an oscillator configured to generate an oscillator signal.

3. The receiver circuit as recited in Claim 2, wherein during a calibration mode of operation the oscillator is configured to operate near a particular frequency in an open loop mode.

4. The receiver circuit as recited in Claim 3, wherein the oscillator is a voltage controlled oscillator.

5. The receiver circuit as recited in Claim 3, wherein the oscillator circuit includes a first divider circuit coupled to divide a frequency of the oscillator signal by a first amount to generate the PLL reference signal.

6. The receiver circuit as recited in Claim 5, wherein the first divider circuit is a power of two ripple divider.

7. The receiver circuit as recited in Claim 5 further comprising a second divider circuit coupled to divide the frequency of the oscillator signal by a second amount to generate the calibration tone.

8. The receiver circuit as recited in Claim 7 wherein the second divider circuit is a programmable divider.

9. The receiver circuit as recited in Claim 7 further comprising a first switch coupled to selectively provide the calibration tone to the IQ mixer during the calibration mode of operation.

10. The receiver circuit as recited in Claim 9, further comprising a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation.

11. The receiver circuit as recited in Claim 9, wherein the first switch is further coupled to selectively provide a receiver RF input signal to the IQ mixer during another mode of operation.

12. The receiver circuit as recited in Claim 11 further comprising an amplifier coupled to amplify the receiver RF input signal prior to mixing in the IQ mixer.

13. The receiver circuit as recited in Claim 1, wherein the IQ mixer generates an in-phase (I) signal and a quadrature (Q) signal that are conveyed through an I channel and a Q channel, respectively, for processing by a baseband circuit.

14. The receiver circuit as recited in Claim 13 further comprising a calibration subsystem coupled to receive representations of the in-phase (I) signal and the quadrature (Q) signal, wherein the calibration subsystem is configured to determine one or more correction parameters for canceling a residual image signal.

15. The receiver circuit as recited in Claim 14 further comprising an analog-to-digital converter coupled to convert the I and Q signals generated by the IQ mixer to digital signals.

16. The receiver circuit as recited in Claim 5, further comprising a switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation.

17. The receiver circuit as recited in Claim 16, wherein during another mode of operation the oscillator is coupled to operate as a transmit oscillator within an offset phase locked loop circuit.

18. A method comprising:

an oscillator circuit generating a calibration tone and a PLL reference signal;

a phase locked loop circuit generating a PLL output signal that is phase locked in relation to the PLL reference signal;

generating quadrature mixer LO signals dependent upon the PLL output signal; and

mixing the calibration tone with the quadrature mixer LO signals.

19. The method as recited in claim 18, further comprising an oscillator of the oscillator circuit operating near a particular frequency in an open loop mode.

20. The method as recited in Claim 18, further comprising dividing a frequency of an oscillator signal generated by the oscillator by a first amount to generate the PLL reference signal.

21. The method as recited in Claim 20, further comprising dividing the frequency of the oscillator signal by a second amount to generate the calibration tone.

22. A receiver circuit comprising:

an oscillator means for generating a calibration tone and a PLL reference signal;

a phase locked loop circuit generating a PLL output signal that is phase locked in relation to the PLL reference signal;

means for generating quadrature mixer LO signals dependent upon the PLL output signal; and

means for mixing the calibration tone with the quadrature mixer LO signals.